CLAIM AMENDMENTS

Please amend the claims (~~strikethrough~~ indicating deletion and underline indicating insertion) as follows:

Claim 1 (currently amended):

1. An apparatus for interrogating a data frame, the data frame comprising a plurality of bits, the apparatus comprising:

first logic, the first logic being configured to select a particular bit pattern in the data frame for interrogation;

second logic, the second logic being configured to compare a selected bit comparison value to said bit pattern to produce a comparison result, wherein the second logic is reconfigurable to enable said bit comparison value to be altered; ~~and~~

third logic, the third logic being configured to determine a location to which the comparison result is to be routed, and wherein one of said first, second and third logic is reconfigurable;

fourth logic, the fourth logic being configured to resolve said comparison result into a first single digital value and to output the first single digital value to the third logic for routing by the third logic; and

complex comparison logic, the complex comparison logic being configured to compare the first single digital value from the fourth logic to a second single digital value to produce a complex comparison result.

Claim 2 (original):

2. The apparatus of claim 1, wherein said first logic is reconfigurable to enable said first logic to alter the particular bit pattern selected from the data frame for interrogation.

Claim 3 (original):

3. The apparatus of claim 2, wherein the first logic is reconfigurable in real time.

Claim 4 (canceled)

Claim 5 (currently amended):

5. The apparatus of claim [[4]]1, wherein the second logic is reconfigurable in real time.

Claim 6 (original):

6. The apparatus of claim 1, wherein said third logic is reconfigurable to enable the location to which the comparison result is routed to be altered.

Claim 7 (original):

7. The apparatus of claim 6, wherein the third logic is reconfigurable in real time.

Claim 8 (canceled)

Claim 9 (original):

9. The apparatus of claim 8, further comprising:

fifth logic, the fifth logic being configured to select a particular bit pattern in the data frame for interrogation;

sixth logic, the sixth logic being configured to compare a selected bit comparison value to said particular bit pattern selected by the fifth logic to produce a comparison result; and

seventh logic, the seventh logic being configured to determine a location to which the comparison result produced by the sixth logic is to be routed, wherein one of said fifth, sixth and seventh logic is reconfigurable.

Claim 10 (original):

10. The apparatus of claim 9, wherein said fifth logic is reconfigurable to enable said fifth logic to alter the particular bit pattern selected from the data frame by the fifth logic for interrogation.

Claim 11 (original):

11. The apparatus of claim 9, wherein the sixth logic is reconfigurable to enable said bit comparison value to be altered.

Claim 12 (original):

12. The apparatus of claim 9, wherein said seventh logic is reconfigurable to enable the location to which the comparison result is routed to be altered.

Claim 13 (original):

13. The apparatus of claim 9, wherein said fifth logic is reconfigurable in real time to enable said fifth logic to alter, in real time, the particular bit pattern selected from the data frame by the fifth logic for interrogation.

Claim 14 (original):

14. The apparatus of claim 9, wherein said sixth logic is reconfigurable in real time in real time to enable said bit comparison value to be altered in real time.

Claim 15 (original):

15. The apparatus of claim 9, wherein said seventh logic is reconfigurable in real time to enable the location to which the comparison result is routed to be altered in real time.

Claim 16 (original):

16. The apparatus of claim 9, further comprising:

eighth logic, the eighth logic being configured to resolve said comparison result produced by said sixth logic into a single digital value and to output the single digital value from the eighth logic to the seventh logic for routing by the seventh logic.

Claim 17 (original):

17. The apparatus of claim 16, further comprising ninth logic, the ninth logic being configured to compare the single digital value received by the fourth logic with the single digital value received by the eighth logic to produce a complex comparison result.

Claim 18 (original):

18. The apparatus of claim 16, wherein the first, second, third, fourth, fifth, sixth and seventh logic are comprised in an application specific integrated circuit (ASIC).

Claim 19 (original):

19. The apparatus of claim 18, wherein the ASIC receives programming signals from a programmable processor, and wherein the first, second, third, fifth, sixth and seventh logic are re-configurable via the programming signals received by the ASIC.

Claim 20 (original):

20. The apparatus of claim 18, wherein the apparatus is utilized for interrogating bits data frames that have been formatted in accordance with a particular communications protocol and transmitted to said apparatus.

Claim 21 (original):

21. The apparatus of claim 1, wherein the apparatus is utilized for interrogating bits data frames that have been formatted in accordance with a particular communications protocol and transmitted to said apparatus.

Claim 22 (original):

22. The apparatus of claim 21, wherein the apparatus is incorporated into a network interface device.

Claim 23 (currently amended):

23. A method for interrogating a data frame, the data frame comprising a plurality of bits, the method comprising the step of:

selecting a particular bit pattern in the data frame for interrogation;

comparing a selected bit comparison value to said bit pattern to produce a comparison result, wherein the bit comparison value can be programmably altered; ~~and~~

determining a location to which the comparison result is to be routed, wherein one of the steps of selecting, comparing and determining is performed by logic that is reconfigurable to thereby enable one of said bit pattern, said bit comparison value and said location to be programmably altered;

resolving said comparison result into a first single digital value; and

comparing the first single digital value to a second single digital value to produce a complex comparison result.

Claim 24 (previously presented):

24. The method of claim 23, wherein the particular bit pattern selected from the data frame for interrogation can be programmably altered in real time.

Claim 25 (previously presented):

25. The method of claim 23, wherein the bit comparison value can be programmably altered in real time.

Claim 26 (previously presented):

26. The method of claim 23, wherein the location to which the comparison result is routed can be programmably altered in real time.

Claim 27 (original):

27. The method of claim 26, further comprising the step of:

prior to determining step, resolving said comparison result into a single digital value such that the comparison result that is routed is the single digital value.

Claim 28 (original):

28. The method of claim 27, wherein the method is performed by an application specific integrated circuit (ASIC) that receives programming signals from a programmable processor, and wherein the programming signals programmably alter the particular bit pattern selected from the data frame for interrogation, the selected bit comparison value compared to said bit pattern, and the location to which the comparison result is routed.

Claim 29 (original):

29. The method of claim 28, wherein the ASIC is incorporated into a network interface card and is utilized for interrogating bits of data frames that have been formatted in accordance with a particular communications protocol.